

Title : Semiconductor Spin Shuttling for High-Speed Quantum Gates and Reconfigurable Connectivity

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High-connectivity architectures, essential for quantum error correction (QEC), can be realized in semiconductors by physically shuttling spin qubits, leveraging established fabrication for large-scale integration. In this work, we use conveyor-mode transport, where gate voltages create traveling potentials in a Si/SiGe quantum dot array, to demonstrate several advancements. We first show high-fidelity (99.5%) spin shuttling over effective 10 μm and $\sim 99\%$ CZ gate fidelity between mobile qubits. Next, we harness the shuttling dynamics itself for computation, realizing a 12 ns Hadamard gate (99.88% fidelity) and selectable CZ/CX gates within a single shuttling step. Finally, we introduce a reconfigurable bus architecture for non-nearest-neighbor connectivity, which we use to perform a four-way quantum non-demolition (QND) parity readout, a key QEC building block. These results elevate spin shuttling from mere transport to a versatile tool for high-speed control and scalable quantum processors.